## What is claimed is:

1. A process of manufacturing a semiconductor device comprising: forming an insulating layer above a semiconductor layer;

forming a conductive layer including at least one of a tantalum layer and a tantalum nitride layer; and

etching the conductive layer by using a gas including SiCl<sub>4</sub> and NF<sub>3</sub>.

2. A process of manufacturing a semiconductor device comprising: forming an insulating layer above a semiconductor layer;

forming a conductive layer including at least one of a tantalum layer and a tantalum nitride layer;

etching the conductive layer by using a gas including NF  $_{\rm 3}$  and fluorocarbon; and

etching the conductive layer by using a gas including SiCl<sub>4</sub> and NF<sub>3</sub>.

- 3. The process of manufacturing a semiconductor device claimed in claim 1 or claim 2 wherein; the ratio of the flow rate of the NF<sub>3</sub> to the flow rate of the sum of the SiCl<sub>4</sub> and the NF<sub>3</sub> is approximately 1 to approximately 30 %.
- 4. The process of manufacturing a semiconductor device claimed in claim 1 or claim 2 wherein; the insulating layer includes at least one of silicon oxide, silicon nitride and silicon oxynitride.
  - 5. A process of manufacturing a semiconductor device comprising: forming an insulating layer above a semiconductor layer;

forming a first tantalum nitride layer, body centered cubic lattice phase tantalum layer and a second tantalum nitride layer in this order;

forming a gate electrode by etching the first tantalum nitride layer, the body centered cubic lattice phase tantalum layer and the second tantalum nitride layer with using a gas including SiCl<sub>4</sub> and NF<sub>3</sub>; and

forming first and second impurity layers constituting a source region and a drain region through introducing a impurity into the semiconductor layer.

- 6. The process of manufacturing a semiconductor device claimed in claim 5, wherein: the ratio of the flow rate of NF 3 to the flow rate of the sum of SiCl<sub>4</sub> and NF 3 is approximately 1 to approximately 30%.
- 7. A process of manufacturing a semiconductor device, as set forth in claim 1, wherein conductive layer is etched to be substantially vertical.
- 8. A process of manufacturing a semiconductor device, as set forth in claim 2, wherein conductive layer is etched to be substantially vertical.
  - 9. A process of manufacturing a semiconductor device, as set forth in claim 5, wherein conductive layer is etched to be substantially vertical.
  - 10. A process of manufacturing a semiconductor device as set forth in claim 7, wherein an angle between the etched conductive layer and the insulating layer is approximately 85 to approximately 90 degrees.
  - 11. A process of manufacturing a semiconductor device as set forth in claim 2, wherein an angle between the etched conductive layer and the insulating layer is approximately 85 to approximately 90 degrees.
  - 12. A process of manufacturing a semiconductor device as set forth in claim 5, wherein an angle between the etched conductive layer and the insulating layer is approximately 85 to approximately 90 degrees.